FRIEDRICH-ALEXANDER
UNIVERSITÄT
ERLANGEN-NÜRNBERG

TECHNISCHE FAKULTÄT

Elektrotechnik-Elektronik-Informationstechnik

EEI KOLLOQUIUM

Chip Assembly Technologies and Codesign Methodology for SiP Products

Dr. Thomas Brandtner
Infineon Technologies, Villach, Österreich

Freitag der 01.02.2019, 10^{30} Uhr
Tennenlohe, Wetterkreuz 15, Raum 00.099

Diskussionsleitung: Prtof. Dr.-Ing. R. Weigel

- Introduction
- Basic Challenges in Chip Assembly
- More-than-Moore, Interconnect Gap, Thermal Expansion, Reliability
- Overview on Package Platforms
- Laminate / BGA Packages
  High-density Interconnects, Flip-chip, Bumps, Copper Pillars
- Chip-Embedding, Wafer-Level-Packages
  Infineon eWLB, TSMC InFo, Chip-embedding in Laminate
- 3D IC & Silicon integration
  Package-on-Package, Thru-Silicon-Via, 2,5D Interposer, Intel EMIB, LETI CoolCube
- Product Examples
  Apple A12, Apple S3, Intel Stratix, Nvidia Pascal
- Chip/Package Codesign Methodology
  - o Distributed Teams – Data Exchange with “Standard” File Formats
  - o Assembly Design Kits
  - o Common Layout Environment in Cadence Virtuoso
- Conclusion